Customer No.: 31561
Application No.: 10/064,644
Docket NO.: 9223-US-PA

In The Claims:

Claims 1-15 (Cancelled)

16. (currently amended) A flip chip die for joining with a flip-chip package substrate, wherein the flip chip die having an active surface thereon, comprising:

a group of core die pads on the active surface; and

a plurality of die pad rows on the active surface sequentially laid outside the ~~ground~~ group of core die pads such that one end of each of the die pad rows is adjacent to the group of core die pads and each die pad row includes a plurality of die pads therein, wherein the die pad rows are selected from signal die pad rows, power die pad rows and ground die pad rows.

17. (currently amended) The flip chip die of claim 16, wherein the group of core die pads includes a plurality of core power die pads and core ground die pads.

18. (currently amended) The flip chip die of claim 16, wherein at least one signal die pad row is positioned between the power die pad row and the ground die pad row.

19. (currently amended) A flip chip die for joining with a flip-chip package substrate, wherein the die having an active surface thereon, ~~flip-chip package substrate~~ comprising:

~~a plurality of patterned conductive layers sequentially stacked over each other;~~

~~at least one insulation layer between two neighboring conductive layers for isolating the conductive layers electrically such that the insulation layer alternates in position with the conductive layer; and~~

~~at least one conductive plug passing through the insulation layer for electrically connecting the conductive layers;~~

~~wherein the upper most conductive layer further includes:~~

~~a group of core bump pads;~~

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~~a plurality of inner bump pad rows sequentially laid outside a group of core bump pads, wherein a first end of each of the inner bump pad rows are adjacent to the group of core bump pads with each inner bump row having a plurality of inner bump pads therein, and the inner bump pad rows are selected from signal bump pad rows, power bump pad row and ground bump pad rows; and~~

~~a plurality of outer bump pad rows sequentially laid outside a second end of each of the inner bump pad rows with each outer bump pad row having a plurality of outer bump pads thereon and the outer bump pad rows labeled sequentially as a first outer bump pad row, a second outer bump pad row and a third outer bump pad row from inside to outside, wherein the shortest distance between the neighboring outer bump pads within the second outer bump pad row is wide enough to permit the passage of at least one conductive trace, the shortest distance between the outer bump pad within the second outer bump pad row and the outer bump pad within the third outer bump pad row is wide enough to permit the passage of at least one conductive trace, and the shortest distance between the neighboring outer bump pads within the third outer bump pad row is wide enough to permit the passage of at least two conductive traces; and~~

~~the flip chip die having an active surface thereon, comprising:~~

a group of core die pads on the active surface ~~that corresponds in position to the group of core bump pads~~;

a plurality of inner die pad rows on the active surface ~~that correspond to the inner bump pad row~~ sequentially laid outside the group of core die pads, wherein a first end of each of the inner die pad rows is adjacent to the group of core die pads and ; ~~wherein~~ each inner die pad row has a plurality of inner die pads therein, wherein ~~that correspond in position to the inner bump padsand~~ the inner die pad rows are selected from signal die pad rows, power die pad rows and ground die pad rows; and

a plurality of outer ~~layer~~ die pad rows on the active surface laid outside a second end of each of the inner die pad rows and vertical to the inner die pad rows ~~that correspond in position to the outer bump pad rows~~, wherein each outer die pad row

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has a plurality of outer die pads therein~~that correspond in position to the outer bump pads~~.

20. (currently amended) The flip chip die of claim 19, wherein ~~the group of core bump pads includes a plurality of core power bump pads and core ground bump pads and~~ the group of core die pads includes a plurality of core power ~~bump~~die pads and core ground die pads ~~that correspond in position to the core power bump pads and core ground bump pads~~.

21. (currently amended) The flip chip die of claim 19, wherein at least one signal die pad row is positioned between the power die pad row and the ground die pad row in the inner die pads rows.

22. (currently amended) The flip chip die of claim 19, wherein the outer die pads are signal die pads.

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23. (new) The flip chip die of claim 16, wherein each die pad has a bump thereon.

24. (new) The flip chip die of claim 16, wherein the flip-chip package substrate is a multi-layer substrate and has a plurality bump pads at a surface of the package substrate corresponding to the die pads of the flip chip die respectively.

25. (new) The flip chip die of claim 19, wherein each die pad has a bump thereon.

26. (new) The flip chip die of claim 19, wherein the flip-chip package substrate is a multi-layer substrate and has a plurality bump pads at a surface of the package substrate corresponding to the die pads of the flip chip die respectively.

27. (new) The flip chip die of claim 19, wherein the outer die pad rows includes a first outer die pad row, a second outer die pad row and a third die bump pad row sequentially from inside to outside, wherein the shortest distance between the

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neighboring outer die pads of the second outer die pad row is wide enough to permit the passage of at least one conductive trace at a surface of the package substrate, the shortest distance between the outer die pad of the second outer die pad row and the outer die pad of the third outer die pad row is wide enough to permit the passage of at least one conductive trace at a surface of the package substrate, and the shortest distance between the neighboring outer die pads of the third outer die pad row is wide enough to permit the passage of at least two conductive traces at the surface of a package substrate.

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Response to 35 U.S.C. 121

The Examiner issued a restriction requirement. According to the Office Action, there are at least two patentably distinct species in the claimed invention and a restriction to one of these species in claims is required under 35 U.S.C. 121.

Applicant elects one of the species related to a flip chip die specified in claims 16-22. Applicant adds new claims 23-27 to further define the invention. Applicant also reserves the right to purse the subject matter of the non-elected claims in a divisional application if Applicants so choose.

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CONCLUSION

In view of the foregoing, claims 16-27 remain pending in the application. Favorable consideration and allowance of the present application and all pending claims are hereby courteously requested. In the event a telephone conversation would expedite the prosecution of this application, the Examiner is encouraged to contact the undersigned attorney to discuss the application.

Respectfully submitted,

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